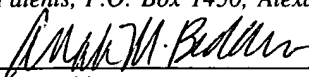


PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



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Angela M. Beddawi

Applicant : Tarek Kaylani et al.
Application No. : 10/789,546
Filed : February 27, 2004
Title : SYNCHRONIZING METHOD AND APPARATUS

Grp./Div. : unknown
Examiner : unknown

Docket No. : 51994/LTR/B600

INFORMATION DISCLOSURE STATEMENT
FOR A CONTINUING NON-CPA APPLICATION

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Post Office Box 7068
Pasadena, CA 91109-7068
April 1, 2004

Commissioner:

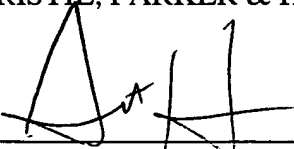
In compliance with the duty of disclosure under 37 CFR §§ 1.56, 1.97 and 1.98, enclosed is FORM PTO/SB/08A/B.

The references listed thereon are not enclosed because they were of record in the parent application, Application No. 09/498,162, filed February 4, 2000.

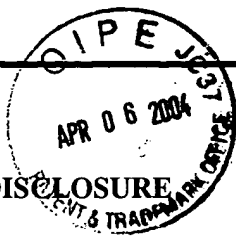
It is respectfully requested that these references be considered in the examination of this application, and identified in the list of references cited on the patent issuing on this application.

Respectfully submitted,

CHRISTIE, PARKER & HALE, LLP

By  Reg # 41,057
LeRoy T. Rahn
Reg. No. 20,356
626/795-9900

LTR/amb
Enclosure
AMB PAS558565.1-*04/1/04 11:00 AM



**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(use as many sheets as necessary)

Attorney Docket Number	51994/LTR/B600
Application Number	10/789,546
Filing Date	February 27, 2004
Applicant(s)	Tarek Kaylani et al.
Group Art Unit	unknown
Examiner Name	unknown

U.S. PATENT DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	DOCUMENT NUMBER Number - Kind Code ² (If Known)	PUBLICATION DATE MM-DD-YYYY	NAME OF PATENTEE
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		5,142,555	08-25-1992	Whiteside
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		5,493,243	02-20-1996	Ghoshal
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		US 6,463,111 B1	10-08-2002	Upp

OTHER DOCUMENTS

EXAMINER INITIALS	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article, title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.
		D. CHEN, "A Power and Area Efficient CMOS Clock/Data Recovery Circuit for High-Speed Serial Interfaces", IEEE Journal of Solid-State Circuits, Vol. 31, No. 8, August 1996, pages 1170-1176, New York
		D. CHEN et al., "A Single-Chip 266Mb/s CMOS Transmitter/Receiver for Serial Data Communications", Circuits Conference; Digest of Technical Papers; 40 th ISSCC; IEEE International, 1993, pages 100-101, 269
		"Hybrid Analog/Digital Clock Recovery for Burst-Mode-Data", IBM Technical Disclosure Bulletin, US, IBM Corp., New York, Vol. 37, No. 4B, April 1994, pages 407-408

EXAMINER SIGNATURE	DATE CONSIDERED
<p>EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant. ¹Applicant's unique citation designation number (optional). ²See Kinds Codes of USPTO Patent Documents at www.pto.gov or MPEP 901.4. ³Enter Office that issued the document, by the two-letter code (WIPO standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁶Applicant is to place a check mark here if English Language Translation is attached.</p>	